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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,539	09/23/2003	Linhai He		2127

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,539	HE ET AL.	
	Examiner	Art Unit	
	Derrick W. Ferris	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-20,22 and 23* is/are rejected.

7)☒ Claim(s) *5,21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. This application is a continuation of application 09/264,834. Applicant did not address the final rejection for the parent case; however, the applicant did clean up the claims with respect to provisioning of a shared buffer. The examiner still maintains the rejection given these minor changes to the claims. As such, the rejection is included below in the present Office action. In addition, the examiner has supplied a new rejection as mentioned in Final Office action for the parent case based on applicant's further arguments (see comments below with respect to response to amendment).

Response to Amendment

2. **Claims 1-23** as amended filed are still in consideration for this application.

3. Examiner maintains the obviousness rejection to *Worster* in view of *Mitra*. At issues is the limitation:

> *determining effective bandwidth and buffer space requirements from said set of parameters, wherein a ratio of said effective buffer space requirement b_o to said allocated buffer size B_i is substantially equal to a ratio of said effective bandwidth requirement to said link capacity C;*

supported in claim 1, lines 12-15; claim 11, lines 11-14; claim 22, lines 17-20; and claim 23, lines 14-18. Examiner notes this limitation is supported by the cited prior art for the reference as taught in combination. Specifically, *Worster* teaches the comparison of ratios at column 7 for equation (6) when e_0 is equal to r as is known in the art (i.e., when the equation is satisfied for B_T /(B/C) then substitute e_o for r in comparison of the relationships by simple manipulation of the

equations presented in applicant's written disclosure on page 11, line 12, and page 12, line 1). (In other words both equations describe a linear line for a leaky bucket as shown in applicant's figure 7 for buffers in general given a link capacity and effective bandwidth.) In making the comparison, examiner notes that $b_o = B_T$, and $B_i = B$ (i.e., in both equations the effective bandwidth is e_o and the link bandwidth capacity are disclosed). Thus in general, the equality is known in the art for a linear part of a leaky bucket. Examiner notes that it would have been obvious to a skilled artisan prior to applicant's invention to also base the same equation on an individual buffer for a shared buffer space as is known in the art (to obtain b_o and B_i) based on the combined teachings of *Worster* in view of *Mitra* where *Mitra* discloses determining the allocation of memory space for each output port for a shared buffer space thus providing a motivation (i.e., *Mitra* discloses individual memory space for an intended output port I [column 7, lines 39-40]).

In addition, with respect to applicant's previous arguments, the examiner has added a new rejection to better show the examiner's reasoning in rejecting the claims. In particular, an effective bandwidth for a *single* output buffer is well known in the art as admitted by applicant and as further taught by *Elwaid*. Applicant appears to modify the *Elwaid* reference to teach an effective bandwidth requirement for *multiple* output ports sharing the same buffer (i.e., a common buffer is partitioned into a partition corresponding to each output port where the effective bandwidth is found for each partition or subqueue). Examiner notes such a modification would have been obvious in view of the prior art. In particular, applicant attempts to argue the following equation:

$$\Sigma B_i = B_{SMF}$$

This equation is supported at least at page 14, lines 16-21 of applicant's specification. In particular, *Elwaid* teaches B_i for a single output port (i.e., a single partition). Thus combing multiple output ports that share a common buffer would result in the summation of the allocated buffer sizes of B_i to B_N which is B_{SMF}. Thus the concept of the above equation, which is what applicant attempts to argue, would have been obvious as taught by references in combination (e.g., see rejection below).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-4,6-20, and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,028,840 to *Worster* in view of U.S. Patent No., 5,909,547 to *Mitra*.

As to **claim 1**, *Worster* discloses a method and apparatus for connection admission control (CAC) for various service types including variable bit rate (VBR) traffic in an ATM network. Disclosed by the reference are the general steps of receiving a signal representing a request for admission of a virtual circuit, determining the effective bandwidth and buffer space from a set of parameters and admitting a virtual circuit if the determined bandwidth and buffer space requirements are less than the available buffer memory space for a buffer in general (i.e., the patent incorporates the two-phase approach as disclosed by *Elwalid* in reference to Applicant's written disclosure on pages 3, lines 5-14). In addition, with respect to applicant's figure 2 and traffic shaping, examiner notes

that *Worster* also discloses that buffer and leaky-bucket usage is well known in the art [column 1, lines 37-42].

Examiner notes that the reference is generally silent on both the location and the type of buffer memory used. Specifically, shown in figure 7 the buffer memory 18(a)-18(d) appears on each card [column 11, lines 16-20] where it is unclear if this memory is shared and allocated to various output ports. Thus the reference is deficient to the claim limitation of "*allocating a portion, B_i of said buffer to each of said output ports*" [e.g., claim 1, line 5; and Applicant's written disclosure for emphasis on page 3, lines 22-24 with respect to the problem that the applicant is trying to solve]. Examiner notes that such a claim limitation of allocating a portion of the buffer to each of the output ports would have been obvious to a skilled artisan prior to applicant's invention. Examiner notes that a motivation would be to provide a more enhanced efficiency in multi-port network nodes as is known in the art and as supported by *Mitra* on column 3, lines 1-3. In addition to disclosing a network of nodes including an access regulators shown in figure 1, *Mitra* discloses provisionally allotted memory space B_i for an intended output port I [column 7, lines 38-40].

As both references disclose ATM networking in general, and more specifically ATM networking using virtual circuits and admissions control, examiner notes a strong motivation to combine the subject matter as a whole for both references.

As to **claim 2**, *Worster* discloses using set parameters such as a lossless effective bandwidth [column 3, lines 20-24; column 7, lines 1-8].

As to **claim 3**, *Worster* discloses using set parameters such as a lossless effective [column 7, lines 20-25].

As to **claim 4**, *Mitra* discloses a shared bandwidth approach [column 9, lines 25-30; column 10, lines 1-24]

As to **claim 6**, *Worster* discloses leaky bucket regulators in general and *Mitra* discloses using leaky bucket regulators for access regulators [column 4, lines 43-53].

As to **claims 7 and 8**, in addition to the reasoning supplied in claim 1, *Mitra* discloses the step of allocating the effective bandwidth requirement in the link to the admitted virtual circuit [column 3, lines 14-19].

As to **claims 9 and 10**, figure 4 step 445 of *Mitra* shows a broad but reasonable interpretation of allocating the effective buffer space requirement in said node for said admitted circuit. This is also disclosed in column 9, lines 25-67 and column 10, lines 1-23].

As to **claim 11**, see the combined reasoning behind the rejection of claims 1 and 2.

As to **claim 12**, see the reasoning behind the rejection for claim 8.

As to **claim 13**, see the reasoning behind the rejection for claim 1 and also column 7, lines 36-38.

As to **claims 14 and 15**, see the reasoning behind the rejection for claim 6.

As to **claim 16**, see the reasoning behind the rejection for claim 7.

As to **claims 17 and 18**, see the reasoning behind the rejection for claim 9.

As to **claim 19**, see the reasoning behind the rejection for claim 3.

As to **claim 20**, see the reasoning behind the rejection for claim 4.

As to **claims 22**, see the reasoning behind the rejection for claim 1.

As to **claims 23**, see the reasoning behind the rejection for claim 11.

6. **Claims 1-4,6-20, and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over "A New Approach for Allocating Buffers and Bandwidth to Heterogeneous, Regulated Traffic in an ATM Node" to *Elwalid et al.* ("*Elwalid*") in view of U.S. Patent No., 5,757,771 A B1 to *Li et al.* ("*Li*").

As to **claim 1**, *Elwalid* discloses allocating a bandwidth for *a single* output queue, see e.g., figure 1 (i.e., *Elwalid* discloses B_i for a single output port). Thus *Elwalid* teaches a step of provisioning, receiving, determining and admitting for a single output port using a single queue. In addition, *Elwalid* also teaches determining the ratios as recited for a single output subqueue as part of equation 11 on page 1118.

Elwalid is silent or deficient to the concept of partitioning a common queue into subqueues where each subqueue is dedicated to a specific out port (i.e., *Elwalid* teaches the concept of one subqueue in a common buffer and not multiple subqueues for a common buffer and where the effective bandwidth is found for each partition or subqueue).

Li teaches the above-mentioned limitation in e.g., the abstract. In particular, *Li* teaches that a common queue can be partitioned into subqueues, one for each output, where size of the subqueue changes dynamically.

Examiner purposes to modify *Elwalid* to teach multiple subqueues such that the effective bandwidth may be found for each subqueue or partition.

Hence examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to include a common buffer where a portion of the buffer is provisioned for each output port for use in a computation of effective bandwidth. In particular, one skilled in the art would be motivated to partition a common queue in order to reduce costs associated with using individual and independent queues. Examiner notes a reasonable expectation of success to combine both references since both references teach transporting ATM VBR traffic.

As to **claim 2**, see equation 15 on page 1118 of *Elwalid.*

As to **claim 3**, see e.g., bottom left of page 1118 of *Elwalid.*

As to **claim 4**, $\Sigma B_i = B_{SMF}$ is taught as a function of each subqueue as mentioned in the rejection for claim 1.

As to **claim 6**, *Elwalid* teaches a leaky bucket regulator, see e.g., right-hand column of page 1115.

As to **claim 7**, *Elwalid* teaches allocating the bandwidth for each virtual circuit for each output port individually.

As to **claim 8**, see e.g., equation 12 on page 1118 of *Elwalid.*

As to **claim 9**, *Elwalid* teaches allocating the bandwidth for each virtual circuit for each output port individually.

As to **claim 10**, *Li* teaches that the subqueue lengths cannot exceed the length of the common buffer.

As to **claim 11**, see the combined reasoning behind the rejection of claims 1 and 2.

As to **claim 12**, see the reasoning behind the rejection for claim 8.

As to **claim 13**, see the reasoning behind the rejection for claim 1 and also column 7, lines 36-38.

As to **claims 14 and 15**, see the reasoning behind the rejection for claim 6.

As to **claim 16**, see the reasoning behind the rejection for claim 7.

As to **claims 17 and 18**, see the reasoning behind the rejection for claim 9.

As to **claim 19**, see the reasoning behind the rejection for claim 3.

As to **claim 20**, see the reasoning behind the rejection for claim 4.

As to **claims 22**, see the reasoning behind the rejection for claim 1.

As to **claims 23**, see the reasoning behind the rejection for claim 11.

Allowable Subject Matter

7. **Claims 5 and 21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (571) 272-3123. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

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9/17/04